+8..24V Unregulated power supply IN		V++	C1
Input to PLD (not used)	*	CNTL2	C2
Reset OUTPUT (active low)	*	_RESET	C3
Reset INPUT (active low)	*	_RESIN	C4
Databus bit D7		AD7	C5
Databus bit D6		AD6	C6
Databus bit D5		AD5	C7
Databus bit D4		AD4	C8
Databus bit D3		AD3	C9
Databus bit D2		AD2	C10
Databus bit D1		AD1	C11
Databus bit D0		AD0	C12
XIRQ input (active low)	*	_XIRQ	C13
IRQ input (active low)	*	_IRQ	C14
Port E bit7		PE7	C15
Port E bit6		PE6	C16
Port E bit5		PE5	C17
Port E bit4		PE4	C18
Port E bit3		PE3	C19
Port E bit2		PE2	C20
Port E bit1		PE1	C21
Port E bit0		PE0	C22
Port A bit0 (also SWITCH PA0 and/or DTR)	*	PA0	C23
Port A bit1 (also SWITCH PA1)	*	PA1	C24
Port A bit2	*	PA2	C25
Port A bit3	*	PA3	C26
Port A bit4		PA4	C27
Port A bit5 (also LED1)		PA5	C28
Port A bit6 (also LED2)		PA6	C29
Port A bit7	*	PA7	C30
+5V Regulated power supply OUT		Vcc	C31
GND		GND	C32

*) signal has on-board pull-up 10k to Vcc

A1	PPA0	*	Address bus bit A0
A2	PPA1	*	Address bus bit A1
A3	PPA2	*	Address bus bit A2
A4	PPA3	*	Address bus bit A3
A5	PPA4	*	Address bus bit A4
A6	PPA5	*	Address bus bit A5
A7	PPA6	*	Address bus bit A6
A8	PPA7	*	Address bus bit A7
A9	R/_W		Read/Write
A10	TMS	*	JTAG (reserved)
A11	TCK	*	JTAG (reserved)
A12	LCD	*	LCD enable (active high)
A13	_LATCH0	*	Latch0 select (active low)
A14	_LACTH1	*	Latch1 select (active low)
A15	TDI	*	JTAG (reserved)
A16	TDO	*	JTAG (reserved)
A17	_LATCH2	*	Latch2 select (active low)
A18	E		E clock
A19	PPB0	*	PSD Port B bit0
A20	PPB1	*	PSD Port B bit1
A21	PPB2	*	PSD Port B bit2
A22	PPB3	*	PSD Port B bit3
A23	PPB4	*	PSD Port B bit4
A24	PPB5	*	PSD Port B bit5
A25	PPB6	*	PSD Port B bit6
A26	PPB7	*	PSD Port B bit7
A27	_LATCH3	*	Latch3 select (active low)
A28	_LATCH4	*	Latch4 select (active low)
A29	_SS	*	SPI Slave Select (active low) (also DSR)
A30	SCK	*	SPI Clock
A31	MOSI	*	SPI Master Out, Slave In
A32	MISO	*	SPI Master In, Slave Out